CDA 4213 001/CIS 6930 012

Fall 2019

# CMOS VLSI Design

Lab 5 Report

Canvas Submission

Due: 11:59 PM, 20th Oct. 2019

You need to submit only report for your team.

Note: Upload PDF version of this report. Only PDF format is accepted.

|  |  |
| --- | --- |
| Today’s Date: |  |
| Your Team and  U Numbers: |  |
| Your U Number: |  |
| No. of Hours Spent: |  |
| Exercise Difficulty:  (Easy, Average, Hard) |  |
| Work Distribution:  (Identify who did what) |  |
| Any Other Feedback: |  |

**Question 1 (5 pts): Positive Level Sensitive D-latch**

Include the following

a) Transistor level diagram

b) Image of your layout

c) Bounding box area (width x height)

d) Waveform results

**Question 2 (5 pts): Positive Edge Triggered D Flip-flop**

Include the following

a) Transistor level diagram

b) Image of your layout

c) Bounding box area (width x height)

d) Waveform results

**Question 3 (10 pts): 3-bit Shift Register**

Include the following

a) Transistor level diagram

b) Image of your layout

c) Bounding box area (width x height)

d) Waveform results